LISTING OF CLAIMS

Claim 1 (Original): A memory device for communicating with an integrated circuit via a communication bus, said device comprising:

an interface circuit for receiving communication signals from the communication bus, and for decoding the communication signals, and for generating a plurality of protocol signals and for outputting one of the plurality of protocol signals in response to a select signal;

a user selectable non-volatile memory for storing user selected protocol and for generating the select signal, corresponding to the user selected protocol;

a non-volatile memory; and

a controller for controlling the non-volatile memory; said controller responsive to said one protocol signal.

Claim 2 (Original): The memory device of claim 1 wherein the interface circuit comprises:

a decoding circuit for receiving the communication signals and for decoding the communication signals to generate a plurality of protocol signals;

a multiplexer for receiving the plurality of protocol signals and for generating one of the plurality of protocol signals in response to a select signal.

Claim 3 (Original): The memory device of claim 2 wherein the plurality of protocol signals represent protocol for LPC communication, FWH communication.

Claim 4 (Original): The memory device of claim 1 wherein the user selectable non-volatile memory comprises a non-volatile fuse.

Claim 5 (Original): The memory device of claim 4 further comprising:

a programming logic circuit for receiving the user selected protocol to program the non-volatile fuse.

Claim 6 (Original): The memory device of claim 5 further comprising:

said non-volatile fuse has an output;

a fuse sense circuit for receiving the output and for generating a fuse control signal;

a latch for receiving the fuse control circuit and for generating the select signal.

Claim 7 (Original): The memory device of claim 6 further comprising:

a mode selecting-circuit responsive to a test signal for testing the memory device or for operating the memory device.

Claim 8 (Original): A memory device for communicating with an integrated circuit via a communication bus, said device comprising:

an interface circuit for receiving communication signals from the communication bus, and for decoding the communication signals, and for generating a plurality of protocol signals, and for outputting one of the plurality of protocol signals in response to a select signal;

a non-volatile fuse for generating the select signal;

a non-volatile memory;

a controller for controlling the non-volatile memory; said controller responsive to said one protocol signal; and

a sensing circuit for detecting the communication signals and for programming the non-volatile fuse.

Claim 9 (Original): The memory device of claim 8 wherein the interface circuit comprises:

a decoding circuit for receiving the communication signals and for decoding the communication signals to generate a plurality of protocol signals;

a multiplexer for receiving the plurality of protocol signals and for generating one of the plurality of protocol signals in response to a select signal.

Claim 10 (Original): The memory device of claim 9 wherein the plurality of protocol signals represent protocol for LPC communication, FWH communication.

STATUS OF THE APPLICATION

- Claims 1-6 and 8-10 are rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,851,014 to *Chang et al.* ("*Chang*") in view of U.S. Patent No. 4,783,606 to *Goetting* ("*Goetting*").
- Claim 7 is rejected under 35 U.S.C. § 103(a) as being unpatentable over *Chang* in view of *Goetting* and in further view of U.S. Patent No. 5,596,538 to *Joo* ("*Joo*").